查询ADN2850供应商



a

# Nonvolatile Memory, Dual 1024 Position Programmable Resistors

## Preliminary Technical Data — ADN2850

### FEATURES

Dual, 1024 Position Resolution
25K, 250K Ohm Full Scale Resistance
Low Temperature Coefficient -- 35ppm/°C
Nonvolatile Memory[1] Preset Maintains Wiper Settings
Wiper Settings Read Back
Linear Increment/Decrement
Log taper Increment/Decrement
SPI Compatible Serial Interface
+3V to +5V Single Supply or ±2.5V Dual Supply
26 bytes User Nonvolatile Memory for Constant Storage with Current Monitoring Configurable Function

### APPLICATIONS

SONET, SDH, ATM, Gigabit Ethernet, DWDM Laser Diode Driver Optical Supervisory Systems

### GENERAL DESCRIPTION

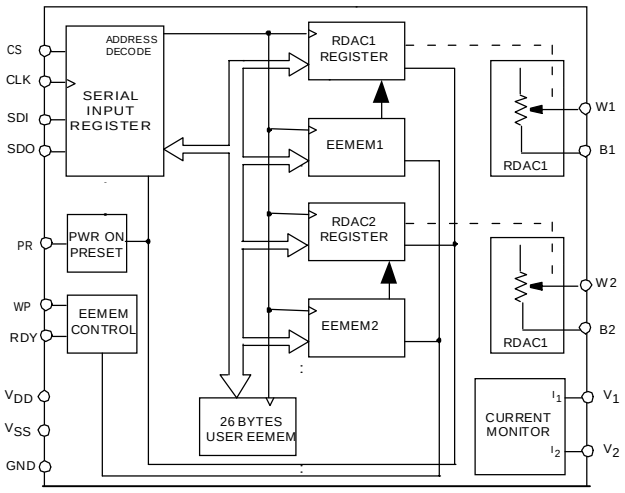
The ADN2850 provides dual channel, digitally controlled programmable resistors[2] with resolution of 1024 positions. These devices perform the same electronic adjustment function as a mechanical rheostat. The ADN2850's versatile programming via a standard serial interface allows sixteen mode of operations and adjustment including scratch pad programming, memory storing and retrieving, increment/decrement, log taper adjustment, wiper setting readback, and extra user defined EEMEM.

In the scratch pad programming mode, a specific setting can be programmed directly to the RDAC[2] register, which sets the resistance between terminals W-and-B. The RDAC register can also be loaded with a value previously stored in the EEMEM[1] register. The value in the EEMEM can be changed or protected. When changes are made to the RDAC register, the value of the new setting can be saved into the EEMEM. Thereafter, such value will be transferred automatically to the RDAC register during system power ON. It is enabled by the internal preset strobe. EEMEM can also be retrieved through direct programming and external preset pin control.

Other key mode of operations include linear step increment and decrement commands such that the setting in the RDAC register can be moved UP or DOWN, one step at a time. For logarithmic changes in wiper setting, a left/right bit shift command adjusts the level in ±6dB steps.

The ADN2850 is available in the 5mm x 5mm LFCSP-16 Lead Frame Chip Scale and thin TSSOP-16 packages. All parts are guaranteed to operate over the extended industrial temperature range of -40°C to +85°C.

### FUNCTIONAL BLOCK DIAGRAM



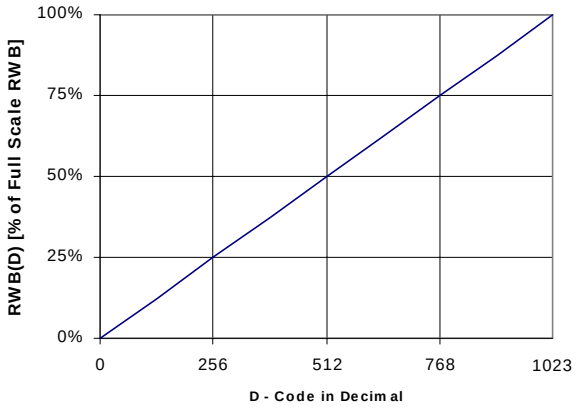




*Figure 1. $R_{WB}(D)$ vs Decimal Code*

Notes:
1. The term nonvolatile memory and EEMEM are used interchangebly
2. The term programmable resistor and RDAC are used interchangebly

REV PrH, 13, AUG 2001

Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices.

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106 U.S.A.
Tel: 617/329-4700 Fax:617/326-8703

**ELECTRICAL CHARACTERISTICS 25K , 250K OHM VERSIONS** ($V_{DD}$ = +3V to +5.5V and, -40°C < $T_A$ < +85°C unless otherwise noted[12].)

| Parameter | Symbol | Conditions | Min | Typ[1] | Max | Units |
|---|---|---|---|---|---|---|
| DC CHARACTERISTICS RHEOSTAT MODE | Specifications apply to all VRs | | | | | |
| Resistor Differential Nonlinearity[2] | R-DNL | $R_{WB}$ | -2 | | +2 | LSB |
| Resistor Integral Nonlinearity[2] | R-INL | $R_{WB}$ | -4 | | +4 | LSB |
| Resistance Temperature Coefficent | $\Delta R_{WB}/\Delta T$ | | | 35 | | ppm/°C |
| Wiper Resistance | $R_W$ | $V_{DD}$ = +5V, $I_W$ = 1V/$R_{WB}$ | | 50 | 100 | Ω |
| | | $V_{DD}$ = +3V, $I_W$ = 1V/$R_{WB}$ | | 200 | | Ω |
| Channel Resistance Matching | $\Delta R_{WB}/R_{WB}$ | Ch 1 and 2 $R_{WB}$, Dx = $3FF_H$ | | 0.2 | | % |
| Nominal Resistor tolerance | $\Delta R_{WB}$ | Dx = $3FF_H$ | -30 | | 30 | % |
| RESISTOR TERMINALS | | | | | | |
| Terminal Voltage Range[3] | $V_{W, B}$ | | $V_{SS}$ | | $V_{DD}$ | V |
| Capacitance[4] Bx | $C_B$ | f = 1 MHz, measured to GND, Code = Half-scale | | 8 | | pF |
| Capacitance[4] Wx | $C_W$ | f = 1 MHz, measured to GND, Code = Half-scale | | 80 | | pF |
| Common-mode Leakage Current [5] | $I_{CM}$ | $V_W = V_B = V_{DD}/2$ | | 0.01 | 1 | µA |
| DIGITAL INPUTS & OUTPUTS | | | | | | |
| Input Logic High | $V_{IH}$ | with respect to GND, $V_{DD}$ = 5V | 2.4 | | | V |
| Input Logic Low | $V_{IL}$ | with respect to GND, $V_{DD}$ = 5V | | | 0.8 | V |
| Input Logic High | $V_{IH}$ | with respect to GND, $V_{DD}$ = 3V | 2.1 | | | V |
| Input Logic Low | $V_{IL}$ | with respect to GND, $V_{DD}$ = 3V | | | 0.6 | V |
| Input Logic High | $V_{IH}$ | with respect to GND, $V_{DD}$ = +2.5V, $V_{SS}$=-2.5V | 2.0 | | | V |
| Input Logic Low | $V_{IL}$ | with respect to GND, $V_{DD}$ = 5V, $V_{SS}$=-2.5V | | | 0.5 | V |
| Output Logic High (SDO, RDY) | $V_{OH}$ | $R_{PULL-UP}$ = 2.2KΩ to +5V | 4.9 | | | V |
| Output Logic Low | $V_{OL}$ | $I_{OL}$ = 1.6mA, $V_{LOGIC}$ = +5V | | | 0.4 | V |
| Input Current | $I_{IL}$ | $V_{IN}$ = 0V or $V_{DD}$ | | | ±1 | µA |
| Input Capacitance[4] | $C_{IL}$ | | | 5 | | pF |
| POWER SUPPLIES | | | | | | |
| Single-Supply Power Range | $V_{DD}$ | $V_{SS}$ = 0V | 3.0 | | 5.5 | V |
| Dual-Supply Power Range | $V_{DD}/V_{SS}$ | | ±2.25 | | ±2.75 | V |
| Positive Supply Current | $I_{DD}$ | $V_{IH} = V_{DD}$ or $V_{IL}$ = GND | | 2 | 20 | µA |
| Programming Mode Current | $I_{DD(PG)}$ | $V_{IH} = V_{DD}$ or $V_{IL}$ = GND | | 35 | | mA |
| Read Mode Current | $I_{DD(READ)}$ | $V_{IH} = V_{DD}$ or $V_{IL}$ = GND | | 3 | | mA |
| Negative Supply Current | $I_{SS}$ | $V_{IH} = V_{DD}$ or $V_{IL}$ = GND, $V_{DD}$ = 2.5V, $V_{SS}$ = -2.5V | | 2 | 20 | µA |
| Power Dissipation[6] | $P_{DISS}$ | $V_{IH} = V_{DD}$ or $V_{IL}$ = GND | | 6 | 110 | µW |
| Power Supply Sensitivity | PSS | $\Delta V_{DD}$ = +5V ±10% | | 0.002 | 0.01 | %/% |
| CURRENT MONITOR Terminals | | | | | | |
| Current Sink at $V_1$[7] | $I_1$ | | 0.0001 | | 10 | mA |
| Current Sink at $V_2$ | $I_2$ | | | | 10 | mA |
| DYNAMIC CHARACTERISTICS[4, 8] | | | | | | |
| Resistor Noise Spectral Density | $e_{N_WB}$ | $R_{WB_FS}$ = 25KΩ / 250KΩ, $T_A$ = 25°C | | 20 / 64 | | nV√Hz |
| Analog Crosstalk ($C_{W1}/C_{W2}$) | $C_T$ | $V_{B1} = V_{B2}$ = 0V, Measured $V_{W1}$ with | | | | |
| | | $V_{W2}$ = 100 mV p-p @ f = 100 kHz, $Code_{1,2} = 200_H$ | | -65 | | dB |

NOTES: See bottom of table next page.

## ELECTRICAL CHARACTERISTICS 25K , 250K OHM VERSIONS ($V_{DD}$ = +3V to +5.5V and, -40°C < $T_A$ < +85°C unless otherwise noted[12].)

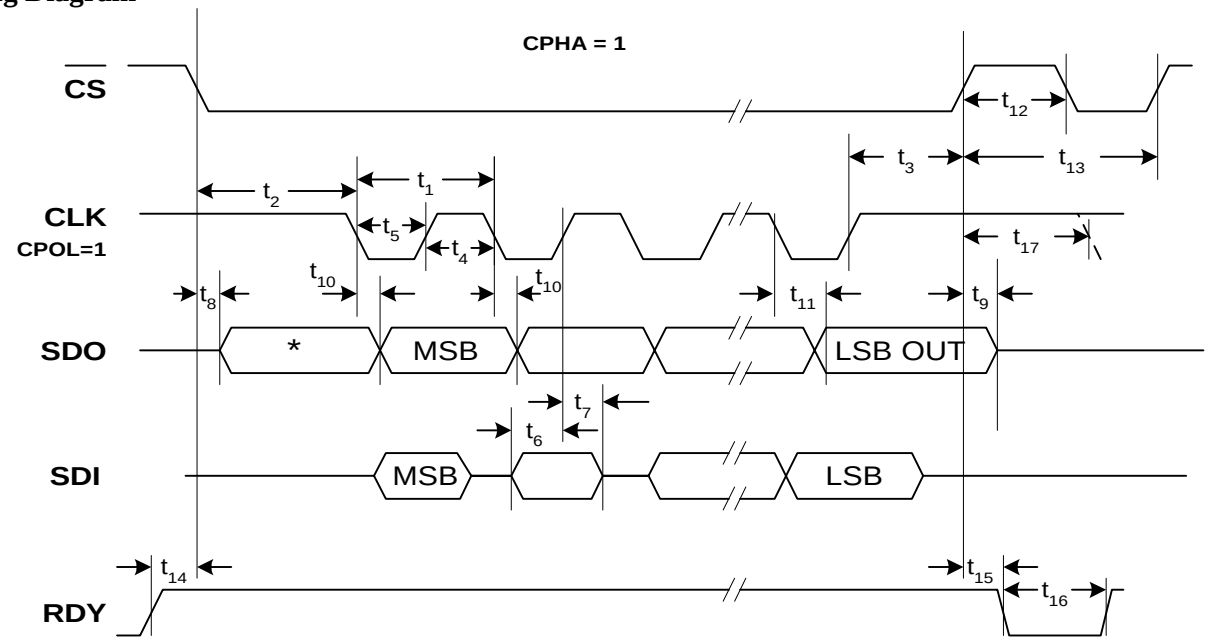
| Parameter | Symbol | Conditions | Min | Typ[1] | Max | Units |
|---|---|---|---|---|---|---|
| INTERFACE TIMING CHARACTERISTICS applies to all parts(Notes 4, 9) | | | | | | |
| Clock Cycle Time ($t_{CYC}$) | $t_1$ | | 20 | | | ns |
| CS Setup Time | $t_2$ | | 10 | | | ns |
| CLK Shutdown Time to CS rise | $t_3$ | | 1 | | | $t_{CYC}$ |
| Input Clock Pulse Width | $t_4$, $t_5$ | Clock level high or low | 10 | | | ns |
| Data Setup Time | $t_6$ | From Positive CLK transition | 5 | | | ns |
| Data Hold Time | $t_7$ | From Positive CLK transition | 5 | | | ns |
| CS to SDO - SPI line acquire | $t_8$ | | | 6 | 40 | ns |
| CS to SDO - SPI line release | $t_9$ | | | 34 | 100 | ns |
| CLK to SDO Propagation Delay[10] | $t_{10}$ | $R_P$ = 2.2KΩ, $C_L$ < 20pF | | 34 | 100 | ns |
| CLK to SDO Data Hold Time | $t_{11}$ | $R_P$ = 2.2KΩ, $C_L$ < 20pF | 0 | | | ns |
| CS High Pulse Width | $t_{12}$ | | 10 | | | ns |
| CS High to CS High | $t_{13}$ | | 4 | | | $t_{CYC}$ |
| RDY Rise to CS Fall | $t_{14}$ | | 0 | 1 | | µs |
| CS Rise to RDY fall time | $t_{15}$ | | | 0.11 | | ms |
| Read/Store to Nonvolatile EEMEM [11] | $t_{16}$ | Applies to Command $2_H$, $3_H$, $9_H$ | | | 25 | ms |
| CS Rise to Clock Edge Setup | $t_{17}$ | | 10 | | | ns |
| Preset Pulse Width (Asynchronous) | $t_{PRW}$ | Not shown in timing diagram | 50 | | | ns |
| Preset Response Time to RDY High | $t_{PRESP}$ | PR pulsed low to refreshed wiper positions | | 70 | | us |
| FLASH/EE MEMORY RELIABILITY[13] | | | | | | |
| Endurance | | | 100,000 | | | Cycles |
| Data Retention[14] | | | | 100 | | Years |

NOTES:

1. Typicals represent average readings at +25°C and $V_{DD}$ = +5V.
2. Resistor position nonlinearity error R-INL is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from ideal between successive tap positions. $I_W$ ~ 50uA for $V_{DD}$= +2.7V and $I_W$ ~ 400uA for $V_{DD}$=+5V. See test circuit figure xxxx
3. Resistor terminals W,B have no limitations on polarity with respect to each other.
4. Guaranteed by design and not subject to production test.
5. Common mode leakage current is a measure of the DC leakage from any terminal B and W to a common mode bias level of $V_{DD}$ / 2.
6. $P_{DISS}$ is calculated from ($I_{DD}$ x $V_{DD}$) + ($I_{SS}$ x $V_{SS}$)
7. Applies to Photo Diode of Optical Receiver.
8. All dynamic characteristics use $V_{DD}$ = +5V and $V_{SS}$ = 0V
9. See timing diagram for location of measured values. All input control voltages are specified with $t_R$=$t_F$=2.5ns(10% to 90% of 3V) and timed from a voltage level of 1.5V. Switching characteristics are measured using both $V_{DD}$ = +3V and +5V.
10. Propagation delay depends on value of $V_{DD}$, $R_{PULL_UP}$, and $C_L$ see applications text.
11. RDY pin low only for commands 2, 3, 8, 9, 10, and PR hardware pulse: CMD_8 ~ 1ms; CMD_9,10 ~0.1ms; CMD_2,3 ~20ms. Device operation at $T_A$=-40ºC & VDD<+3V extends the save time to 35ms.
12. Parts can be operated at +2.7V single supply, except from 0ºC to –40ºC where minimum +3V is needed
13. The ADN2850 contains 16,000 transistors. Die size: 100 mil x 150 mil, 10,500 sq. mil.
14. Retention lifetime equivalent at junction temperature ($T_J$) = 55°C as per JEDEC Std. 22, Method A117. Retention lifetime based on an activation energy of 0.6eV will derate with junction temperature as shown in Figure xxx in the Flash/EE Memory description section of this data sheet.

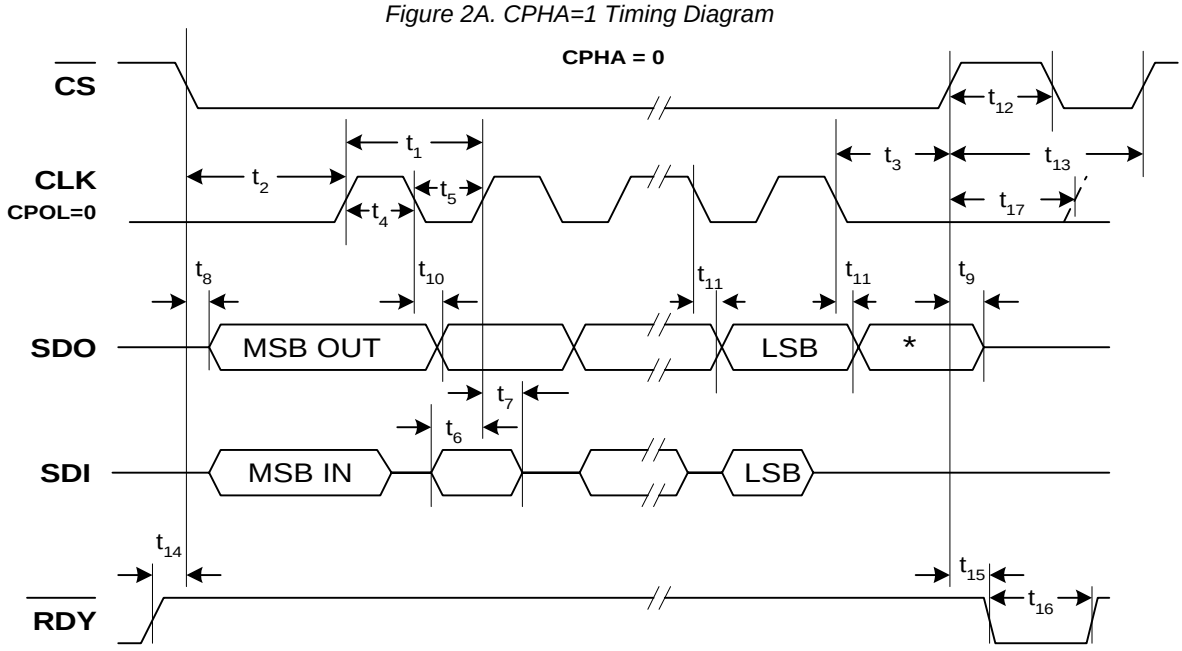
Specifications Subject to Change without Notice

**Timing Diagram**




* Note: Not defined, but normally LSB of character previously transmitted. The CPOL=1 micro controller command aligns the incoming data to the positive edge of the clock.

*Figure 2A. CPHA=1 Timing Diagram*




* Note: Not defined, but normally MSB of character just received. The CPOL=0 micro controller command aligns the incoming data to the positive edge of the clock.

*Figure 2B. CPHA=0 Timing Diagram*

**Absolute Maximum Rating**[1] ($T_A$ = +25°C, unless otherwise noted)

$V_{DD}$ to GND ..... -0.3V, +7V
$V_{SS}$ to GND ..... +0.3V, -7V
$V_{DD}$ to $V_{SS}$ ..... +7V
$V_B$, $V_W$ to GND ..... $V_{SS}$-0.3V, $V_{DD}$+0.3V
$B_X$ – $W_X$ ..... ±20mA
Intermittent[2] ..... ±20mA
Continuous ..... ±1.3mA
Digital Inputs & Output Voltage to GND ..... -0.3V, $V_{DD}$+0.3V
Operating Temperature Range[3] ..... -40°C to +85°C
Maximum Junction Temperature ($T_{J\ MAX}$) ..... +150°C
Storage Temperature ..... -65°C to +150°C
Lead Temperature, Soldering[4]
Vapor Phase (60 sec) ..... +215 °C
Infrared (15 sec) ..... +220 °C
Thermal Resistance Junction-to-Ambient $\theta_{JA}$,
LFCSP-16 ..... 35°C/W
TSSOP-16 ..... 150°C/W
Thermal Resistance Junction-to-Case $\theta_{JC}$,
LFCSP-16 ..... TBD
TSSOP-16 ..... 28°C/W

Package Power Dissipation = ($T_J$MAX - $T_A$) / $\theta_{JA}$

NOTES
1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. Maximum terminal current is bounded by the maximum current handling of the switches, maximum power dissipation of the package, and maximum applied voltage across any two of the B, and W terminals at a given resistance.
3. Includes programming of Nonvolatile memory
4. Applicable to TSSOP-16 only. For LFCSP-16, please consult factory for detail

## Ordering Guide

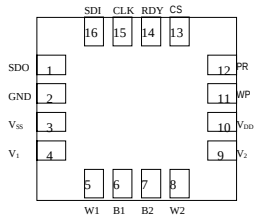
| Model | $R_{WB}$ (k Ohm) | RDNL (LSB) | RINL (LSB) | Temp Range | Package Description | Package Option | Top Mark* |
|---|---|---|---|---|---|---|---|
| ADN2850ACP25 | 25 | ±2 | ±4 | -40/+85°C | LFCSP-16 | CP-16 | ACP25 |
| ADN2850ACP25-RL7 | 25 | ±2 | ±4 | -40/+85°C | LFCSP-16 1500 Pieces 7" Reel | CP-16 | ACP25 |
| ADN2850ACP250 | 250 | ±2 | ±4 | -40/+85°C | LFCSP-16 | CP-16 | ACP250 |
| ADN2850ACP250-RL7 | 250 | ±2 | ±4 | -40/+85°C | LFCSP-16 1500 Pieces 7" Reel | CP-16 | ACP250 |
| ADN2850ARU25 | 25 | ±2 | ±4 | -40/+85°C | TSSOP-16 | RU-16 | ARU25 |
| ADN2850ARU25-REEL7 | 25 | ±2 | ±4 | -40/+85°C | TSSOP-16 1000 Pieces 7" Reel | RU-16 | ARU25 |

* Line 1 contains ADI logo symbol and date code YYWW, line 2 contains product number ADN2850, line 3 branding containing differentiating detail by part type, line 4 contains lot number.

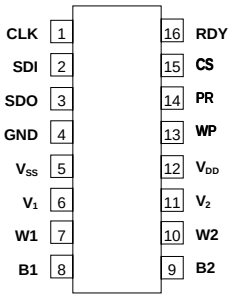
**CAUTION**

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADN2850 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

ADN2850ACP PIN CONFIGURATION




ADN2850ARU PIN CONFIGURATION




## ADN2850ACP PIN DESCRIPTION

| # | Name | Description |
|---|---|---|
| 1 | SDO | Serial Data Output Pin. Open Drain Output requires external pull-up resistor. Commands 9 and 10 activate the SDO output. See Instruction operation Truth Table. Table 2. Other commands shift out the previously loaded SDI bit pattern delayed by 24 clock pulses. This allows daisy-chain operation of multiple packages. |
| 2 | GND | Ground pin, logic ground reference |
| 3 | $V_{SS}$ | Negative Supply. Connect to zero volts for single supply applications. |
| 4 | $V_1$ | Log Output Voltage 1 generated from internal diode configured transistor |
| 5 | W1 | Wiper terminal of RDAC1. ADDR(RDAC1) = $0_H$. |
| 6 | B1 | B terminal of RDAC1 |
| 7 | B2 | B terminal of RDAC2. |
| 8 | W2 | Wiper terminal of RDAC2. ADDR(RDAC2) = $1_H$. |
| 9 | $V_2$ | Log Output Voltage 2 generated from internal diode configured transistor |
| 10 | $V_{DD}$ | Positive Power Supply Pin. |
| 11 | WP | Write Protect Pin. When active low, WP prevents any changes to the present register contents, except PR and cmd 1 and 8 will refresh the RDAC register from EEMEM. |
| 12 | PR | Hardware over ride preset pin. Refreshes the scratch pad register with current contents of the EEMEM register. Factory default loads midscale $512_{10}$ until EEMEM loaded with a new value by the user (PR is activated at the logic high transition). |
| 13 | CS | Serial Register chip select active low. Serial register operation takes place when CS returns to logic high. |
| 14 | RDY | Ready. Active-high open drain output. Identifies completion of commands 2, 3, 8, 9, 10, and PR. |
| 15 | CLK | Serial Input Register clock pin. Shifts in one bit at a time on positive clock edges. |
| 16 | SDI | Serial Data Input Pin. Shifts in one bit at a time on positive clock CLK edges. MSB loaded first. |

## ADN2850ARU PIN DESCRIPTION

| # | Name | Description |
|---|---|---|
| 1 | CLK | Serial Input Register clock pin. Shifts in one bit at a time on positive clock edges. |
| 2 | SDI | Serial Data Input Pin. Shifts in one bit at a time on positive clock CLK edges. MSB loaded first. |
| 3 | SDO | Serial Data Output Pin. Open Drain Output requires external pull-up resistor. Commands 9 and 10 activate the SDO output. See Instruction operation Truth Table. Table 2. Other commands shift out the previously loaded SDI bit pattern delayed by 24 clock pulses. This allows daisy-chain operation of multiple packages |
| 4 | GND | Ground pin, logic ground reference |
| 5 | $V_{SS}$ | Negative Supply. Connect to zero volts for single supply applications. |
| 6 | $V_1$ | Log Output Voltage 1 generated from internal diode configured transistor |
| 7 | W1 | Wiper terminal of RDAC1. ADDR(RDAC1) = $0_H$. |
| 8 | B1 | B terminal of RDAC1 |
| 9 | B2 | B terminal of RDAC2. |
| 10 | W2 | Wiper terminal of RDAC2. ADDR(RDAC2) = $1_H$. |
| 11 | $V_2$ | Log Output Voltage 2 generated from internal diode configured transistor |
| 12 | $V_{DD}$ | Positive Power Supply Pin. |
| 13 | WP | Write Protect Pin. When active low, WP prevents any changes to the present contents except PR and cmd 1 and 8 will refresh the RDAC register from E2MEM. |
| 14 | PR | Hardware over ride preset pin. Refreshes the scratch pad register with current contents of the EEMEM register. Factory default loads midscale $512_{10}$ until EEMEM loaded with a new value by the user (PR is activated at the logic high transition). |
| 15 | CS | Serial Register chip select active low. Serial register operation takes place when CS returns to logic high. |
| 16 | RDY | Ready. Active-high open drain output. Identifies completion of commands 2, 3, 8, 9, 10, and PR. |

Table 1. ADN2850 24-bit Serial Data Word

| | MSB | | | | | | | | | | | | | | | | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RDAC | C3 | C2 | C1 | C0 | 0 | 0 | 0 | A0 | X | X | X | X | X | X | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| EEMEM | C3 | C2 | C1 | C0 | A3 | A2 | A1 | A0 | D 15 | D 14 | D 13 | D 12 | D 11 | D 10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

Command bits are C0 to C3. Address bits are A3-A0. Data bits D0 to D9 are applicable to RDAC whereas D0 to D15 are applicable to EEMEM. Command instruction codes are defined in table 2.

Table 2. ADN2850 Instruction/Operation Truth Table[a,b,d]

| Inst No. | Instruction Byte 0<br>B23 •••••••••••••••• B16<br>C3 C2 C1 C0 A3 A2 A1 A0 | Data Byte 1<br>B15 •••• B8<br>X ••• D9 D8 | Data Byte 0<br>B7 ••• B0<br>D7 ••• D0 | Operation |
|---|---|---|---|---|
| 0 | 0 0 0 0 X X X X | X ••• X X | X ••• X | NOP: Do nothing |
| 1 | 0 0 0 1 0 0 0 A0 | X ••• X X | X ••• X | Write contents of EEMEM(A0) to RDAC(A0) Register). This command leaves device in the Read Program power state. To return part to the idle state, perform NOP instruction #0 |
| 2 | 0 0 1 0 0 0 0 A0 | X ••• X X | X ••• X | SAVE WIPER SETTING: Write contents of RDAC(A0) to EEMEM(A0) |
| 3[e] | 0 0 1 1 << ADDR >> | D15 ••• D8 | D7 ••• D0 | Write contents of Serial Register Data Bytes 0 & 1 to EEMEM(ADDR) |
| 4[c] | 0 1 0 0 0 0 0 A0 | X ••• X X | X ••• X | Decrement 6dB: Right Shift contents of RDAC(A0), steops at all “Zeros”. |
| 5[c] | 0 1 0 1 X X X X | X ••• X X | X ••• X | Decrement All 6dB: Right Shift contents of all RDAC Registers, stops at all “Zeros”. |
| 6[c] | 0 1 1 0 0 0 0 A0 | X ••• X X | X ••• X | Decrement contents of RDAC(A0) by “One”, stops at all “Zero”. |
| 7[c] | 0 1 1 1 X X X X | X ••• X X | X ••• X | Decrement contents of all RDAC Register by “One”, stops at all “Zero”. |
| 8 | 1 0 0 0 0 0 0 0 | X ••• X X | X ••• X | RESET: Load all RDACs with their corresponding EEMEM previously-saved values |
| 9 | 1 0 0 1 << ADDR >> | X ••• X X | X ••• X | Write contents of EEMEM(ADDR) to Serial Register Data Bytes 0 & 1. SDO activated. See Figure xxxx |
| 10 | 1 0 1 0 0 0 0 A0 | X ••• X X | X ••• X | Write contents of RDAC(A0) to Serial Register Data Bytes 0 & 1. SDO activated. See Figure xxxx |
| 11 | 1 0 1 1 0 0 0 A0 | X ••• D9 D8 | D7 ••• D0 | Write contents of Serial Register Data Bytes 0 &1 to RDAC(A0) |
| 12[c] | 1 1 0 0 0 0 0 A0 | X ••• X X | X ••• X | Increment 6dB: Left Shift contents of RDAC(A0), stops at all “Ones”. |
| 13[c] | 1 1 0 1 X X X X | X ••• X X | X ••• X | Increment All 6dB: Left Shift contents of all RDAC Registers, stops at all “Ones”. |
| 14[c] | 1 1 1 0 0 0 0 A0 | X ••• X X | X ••• X | Increment contents of RDAC(A0) by “One”, stops at all “Ones”. |
| 15[c] | 1 1 1 1 X X X X | X ••• X X | X ••• X | Increment contents of all RDAC Register by “One”, stops at all “Ones”. |

NOTES:

a) The SDO output shifts-out the last 24-bits of data clocked into the serial register for daisy chain operation. Exception, following Instruction #9 or #10 the selected internal register data will be present in data byte 0 & 1. Instructions following #9 & #10 must be a full 24-bit data word to completely clock out the contents of the serial register.

b) The RDAC register is a volatile scratch pad register that is refreshed at power ON from the corresponding non-volatile EEMEM register.

c) The increment, decrement and shift commands ignore the contents of the shift register Data Bytes 0 and 1.

d) Execution of the above Operations takes place when the CS strobe returns to logic high.

e) Instruction #3 write two data bytes to EEMEM. But in the cases of addresses 0 and 1, only the last 10 bits are valid for wiper position setting.

## OPERATIONAL OVERVIEW

The ADN2850 programmable resistor is designed to operate as a true variable resistor. The resistor wiper position is determined by the RDAC register contents. The RDAC register acts as a scratch pad register which allows unlimited changes of resistance settings. The scratch pad register can be programmed with any position setting using the standard SPI serial interface by loading the 24-bit data word. The format of the data word is that the first 4 bits are instructions, the following 4 bits are Addresses, and the last 16 bits are data. Once a specific value is set, this value can be saved into a corresponding EEMEM register. During subsequent power up, the wiper setting will automatically be loaded at that value. Saving data to the EEMEM takes about 25ms, and consumes approximately 20mA. During this time the shift register is locked preventing any changes from taking place. The RDY pin indicates the completion of this EEMEM saving process. There are also 13, 2 bytes each of user defined data that can be stored in EEMEM.

## OPERATION DETAIL

There are sixteen instructions which faciliates users' programming needs. Refer to Table 2, the instructions are:

0. Do Nothing
1. Restore EEMEM setting to RDAC
2. Save RDAC setting to EEMEM
3. Save RDAC setting or user data to EEMEM
4. Decrement 6dB
5. Decrement all 6dB
6. Decrement one step
7. Decrement all one step
8. Reset EEMEM setting to RDAC
9. Read EEMEM to SDO
10. Read Wiper Setting to SDO
11. Write data to RDAC
12. Increment 6dB
13. Increment all 6dB
14. Increment one step
15. Increment all one step

### Scratch Pad and EEMEM Programming

The basic mode of setting the programmable resistor wiper position (programming the scratch pad register) is accomplished by loading the serial data input register with the instruction #11, the correponding address, and the data. When the desired wiper position is determined, the user can load the serial data input register with the instruction #2, which stores the setting into the corresponding EEMEM register. After 25ms the wiper position will be stored in the corresponding EEMEM location. If desired, this value can be changed by users in the future or users can set the write-protect to permanently protect the data. Figure 3 provides a programming example listing the sequence of serial data input (SDI) words and the corresponding serial data output (SDO) in hexadecimal format.

| SDI | SDO | Action |
|---|---|---|
| $B00100_H$ | $XXXXXX_H$ | Loads data $100_H$ into RDAC1 register, Wiper W1 moves to 1/4 full-scale position |
| $20xxxx_H$ | $B00100_H$ | Saves copy of RDAC1 register contents into corresponding EEMEM1 register. |
| $B10200_H$ | $20xxxx_H$ | Loads $200_H$ data into RDAC2 register, Wiper W2 moves to 1/2 full-scale position |
| $21xxxx_H$ | $B10200_H$ | Saves copy of RDAC2 register contents into corresponding EEMEM2 register. |

*Figure 3. Set and Save two channels of programmable resistors with independent datas.*

At system power ON, the scratch pad register is refreshed with the value previously saved in the corresponding EEMEM register. The factory preset EEMEM value is midscale. The scratch pad register can also be loaded with the contents of the EEMEM register in three different ways. Executing instruction #1 retrieves the corresponding EEMEM value, executing instruction #8 resets both channels EEMEM values, and pulsing the PR pin also refreshs both EEMEM settings. Operate the PR function however requires a complete pulse signal. When PR goes low, the internal logic sets the wiper at midscale. The EEMEM value will not be loaded until PR returns to high.

### E2MEM Protection

The write-protect (WP) pin provides a hardware EEMEM protection feature which disables any changes of the current content in the scratch pad register at all except commands 1, 8, and PR . Executing these three events cause the EEMEM values restored to the scratch pad registers.

### Linear Increment and Decrement Commands

The increment and decrement commands (#14, #15, #6, #7) are useful for linear step adjustment applications. These commands simplify micro controller software coding by allowing the controller to just send an increment or decrement command to the device. The adjustment can be individual or ganged arrangement. For increment command, executing instruction #14 will automatically move the wiper to the next resistance segment position. The master increment instruction #15 will move all resistor wipers up by one position.

### Logarithmic Taper Mode Adjustment (±6dB/step)

Four programming instructions produce logarithmic taper increment and decrement wiper position control by either individual or ganged arrangement. These settings are activated by the 6dB increment and 6dB decrement instructions #12 & #13 and #4 & #5 respectively. For example, starting at zero scale, executing eleven times of the increment instruction #12 will move the wiper in +6B per step from the 0% of the full scale $R_{WB}$ to the full scale $R_{WB}$. The +6dB increment instruction doubles the value of the RDAC register contents each time the command is executed. When the wiper position is near the maximum setting, the last +6dB increment instruction will cause the wiper to go to the full-scale 1023 code position. Further +6dB per increment instruction will no longer change the wiper position beyond its full scale.

6dB step increment and decrement are achieved by shifting the bit internally to the left and right respectively. The following information explains the nonideal ±6dB step adjustment at certain conditions. Table 3 illustrates the operation of the shifting function on the individual RDAC register data bits. Each line going down the table represents a successive shift operation. Note that the left shift #12 & #13 commands were modified such that if the data in the RDAC register is equal to zero, and the data is left shifted, the RDAC register is then set to code 1. Similary, if the data in the RDAC register is greater than or equal to mid-scale, and the data is left shifted, then the data in the RDAC register is automatically set to full-scale. This makes the left shift function as ideal logarithmic adjustment as is possible.

The right shift #4 & #5 commands will be ideal only if the LSB is zero (i.e. ideal logarithmic - no error). If the LSB is a one then the right shift function generates a linear half LSB error, which translates to a numbers of bits dependent logarithmic error as shown in Figure 4. The plot shows the error of the odd numbers of bits for ADN2850.

Left Shift (+6dB/step)

| Left Shift | Right Shift |
|---|---|
| 00 0000 0000 | 11 1111 1111 |
| 00 0000 0001 | 01 1111 1111 |
| 00 0000 0010 | 00 1111 1111 |
| 00 0000 0100 | 00 0111 1111 |
| 00 0000 1000 | 00 0011 1111 |
| 00 0001 0000 | 00 0001 1111 |
| 00 0010 0000 | 00 0000 1111 |
| 00 0100 0000 | 00 0000 0111 |
| 00 1000 0000 | 00 0000 0011 |
| 01 0000 0000 | 00 0000 0001 |
| 10 0000 0000 | 00 0000 0000 |
| 11 1111 1111 | 00 0000 0000 |
| 11 1111 1111 | 00 0000 0000 |

Right Shift (-6dB/step)

Table 3. Detail Left and Right Shift functions for 6dB step increment and decrement.

Actual conformance to a logarithmic curve between the data contents in the RDAC register and the wiper position for each Right Shift #4 & #5 command execution contains an error only for odd numbers of bits. Even numbers of bits are ideal. The graph in Figure 4 shows plots of Log_Error [i.e. $20*\log_{10}$ (error/code)] ADN2850. For example, code 3 Log_Error=$20*\log_{10}$ (0.5/3)=-15.56dB, which is the worst case. The plot of Log_Error is more significant at the lower codes.

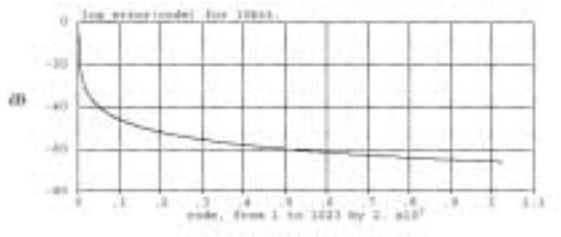


Figure 4. Plot of Log_Error Conformance for Odd Numbers of Bits Only (Even Numbers of Bits are ideal)

**Using Additional internal Nonvolatile EEMEM**

The ADN2850 contains additional internal user storage registers (EEMEM) for saving constants and other 16-bit data. Table 4 provides an address map of the internal storage registers shown in the functional block diagram as EEMEM1, EEMEM2, and 26 bytes of USER EEMEM.

| Address | EEMEM For |
|---|---|
| 0000 | RDAC1[a,c] |
| 0001 | RDAC2 |
| 0010 | USER1[b] |
| 0011 | USER2 |
| : | : |
| 1110 | USER13 |
| 1111 | Factory Reserved |

Table 4: EEMEM Address Map

NOTES:

a) RDAC data stored in EEMEM locations are transferred to their corresponding RDAC REGISTER at Power ON, or when instructions Inst#1, #8, and PR are executed.

b) USER <data> are internal nonvolatile EEMEM registers available to store and retrieve constants and other 16-bit information using Inst#3 and Inst#9 respectively.

**c)** Execution of instruction #1 leaves the device in the Read Mode power consumption state. After the last Instruction #1 is executed, the user should perform a NOP, Instruction #0 to return the device to the low power idling state.

**Daisy Chain Operation**

The serial data output pin (SDO) can be used to readout the content of the wiper settings or EEMEM values under instructions 10 and 9 respectively. If these instructions are not used, SDO can be used for daisy chaining multiple devices for simultaneous operations, see Figure 5. SDO pin contains an open drain N-Ch FET and requires a pull-up resistor if SDO function is used. Users need to tie the SDO pin of one package to the SDI pin of the next package. Users may need to increase the clock period because the pull-up resistor and the capacitive loading at the SDO-SDI interface may induce time delay to the subsequent devices, see Figure 5. If two ADN2850 are daisy chained, this requires total 48 bits of data. The first 24 bits (formatted 4-bit instruction, 4-bit address, and 16-bit data) goes to U2 and the second 24 bits with the same format goes to U1. The CS should be kept low until all 48 bits are clocked into their respective serial registers. The CS is then pulled high to complete the operation.

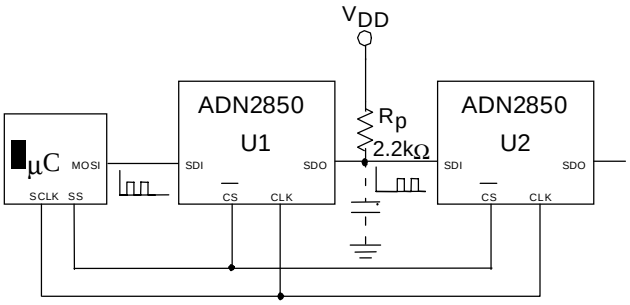



Figure 5. Daisy Chain Configuration

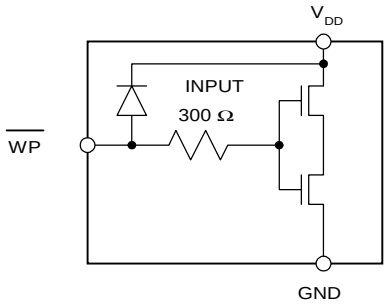



Figure 7B. Equivalent WP Input Protection

**DIGITAL INPUT/OUTPUT CONFIGURATION**

All digital inputs are ESD protected. Digital inputs are high impedance and can be driven directly from most digital sources. For PR and WP, which are active at logic low, should be biased to $V_{DD}$ if they are not used. There are no internal pull-up resistors on any digital input pin. As a result, pull-up resistors are needed if these functions are used.

For SDO and RDY pins, they are open drain digital outputs. Similarly, pull-up resistors are needed if these functions are used. To optimize the speed and power trade off, use 2.2kΩ pull-up resistors.

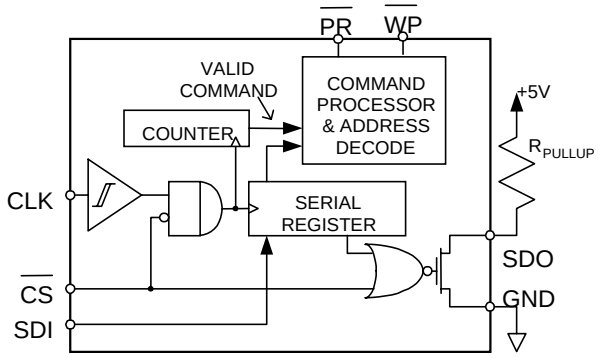



Figure 6. Equivalent Digital Input-Output Logic

The equivalent serial data input and output logic is shown in figure 6. The open drain output SDO is disabled whenever chip select CS is logic high. The SPI interface can be used in two slave modes CPHA=1, CPOL=1 and CPHA=0, CPOL=0..

ESD protection of the digital inputs is shown in figures 7A & 7B.

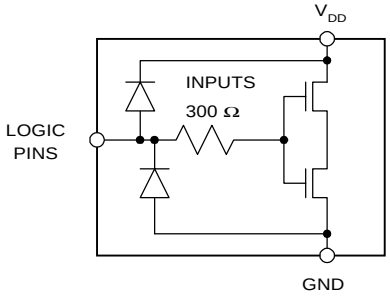



Figure 7A. Equivalent ESD Digital Input Protection

**SERIAL DATA INTERFACE**

The ADN2850 contains a four-wire SPI compatible digital interface (SDI, SDO, CS, and CLK). The 24-bit serial word must be loaded with MSB first, and the format of the word is shown in Table 1. The Command Bits (C0 to C3) control the operation of the programmable resistor according to the instruction shown in Table 2. A0 to A3 are assigned for address bits. A0 is used to address RDAC 1 or RDAC2. Addresses 2 to 14 are accessable by users. Address 15 is reserved for factory usage. Table 4 provides an address map of the EEMEM locations. The Data Bits (D0 to D15) are the values that are loaded into the RDAC register.

The last instruction prior to a period of no programming activity should be applied with the No Operation (NOP), instruction 0. It is recommended to do so to ensure minimum power consumption in the internal logic circuitry

**TERMINAL VOLTAGE OPERATING RANGE**

The ADN2850 positive $V_{DD}$ and negative $V_{SS}$ power supply defines the boundary conditions for proper 2-terminal programmable resistance operation. Supply signals present on terminals W and B that exceed $V_{DD}$ or $V_{SS}$ will be clamped by the internal forward biased diodes, see Figure 8.

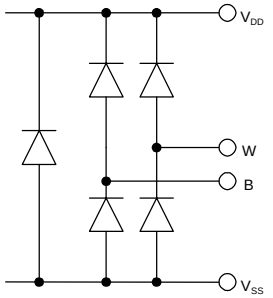



Figure 8. Maximum Terminal Voltages Set by $V_{DD}$ & $V_{SS}$

The ground pin of the ADN2850 device is primarily used as a digital ground reference, which needs to be tied to the PCB's common ground. The digital input contol signals to the ADN2850 must be referenced to the device ground pin (GND), and satisfy the logic level defined in the specification table of this data sheet. An internal level shift circuit insures that the common mode voltage range of the 2-terminals extends from $V_{SS}$ to $V_{DD}$ irrespective of the digital input level.

## RDAC STRUCTURE

The RDAC contains a string of equal resistor segments, with an array of analog switches, that act as the wiper connection. The number of positions is the resolution of the device. The ADN2850 has 1024 connection points allowing it to provide better than 0.1% set-ability resolution. Figure 8 shows an equivalent structure of the connections between the two terminals that make up one channel of the RDAC. The $SW_B$ will always be ON, while one of the switches SW(0) to SW($2^N$-1) will be ON one at a time depending on the resistance position decoded from the Data Bits. Since the switch is not ideal, there is a 50Ω wiper resistance, $R_W$. Wiper resistance is a function of supply voltage and temperature. The lower the supply voltage, the higher the wiper resistance. Similarly, the higher the temperature, the higher the wiper resistance. $R_W$ is the sum of the resistance of SW(D) + SWB from Wiper-to-B terminals Users should be aware of the contribution of the wiper resistance when accurate prediction of the output resistance is needed.

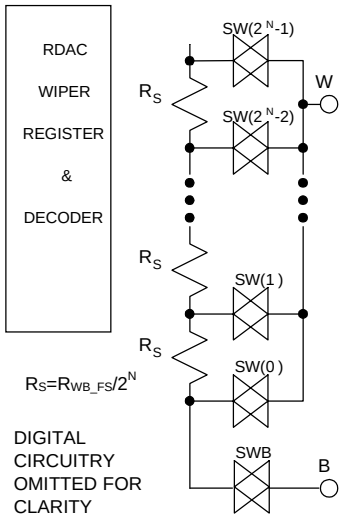



Figure 9. Equivalent RDAC structure

Table 5. Nominal individual segment resistor values

| Device Resolution | 25 KΩ Version | 250 KΩ Version |
|---|---|---|
| 10-Bit | 24.4 Ω | 244 Ω |

## CALCULATIING THE PROGRAMMABLE RESISTANCE

The nominal full scale resistance of the RDAC between terminals W-and-B, $R_{WB_FS}$, are available with 25KΩ and 250KΩ with 1024 positions (10-bit resolution). The final digits of the part number determine the nominal resistance value, e.g., 25KΩ = 25; 250KΩ = 250.

The 10-bit data word in the RDAC latch is decoded to select one of the 1024 possible settings. The following discussion describes the calculation of resistance $R_{WB}(D)$ at different codes of a 25KΩ part. The wiper first connection starts at the B terminal for data $000_H$. $R_{WB}$ is 50Ω because of the wiper resistance and it is independent to the full-scale resistance. The second connection is the first tap point where $R_{WB}(1)$ becomes 24.4Ω+50=74.4Ω for data $01_H$. The third connection is the next tap point representing $R_{WB}(2)$=48.8+50=98.8Ω for data $02_H$ and so on. Each LSB data value increase moves the wiper up the resistor ladder until the last tap point is reached at $R_{WB}(1023)$=25026Ω. See Figure 9 for a simplified diagram of the equivalent RDAC circuit.

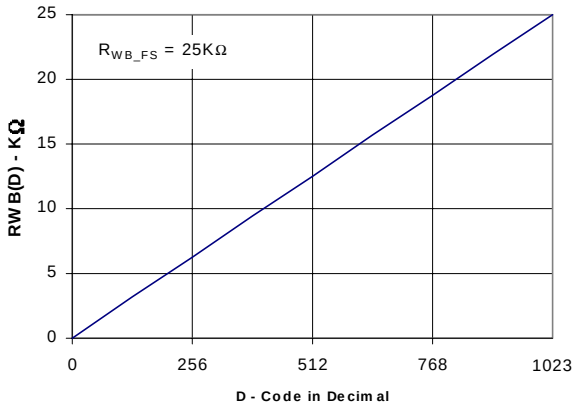



Figure 10. $R_{WB}(D)$ vs Code

The general equation, which determines the programmed output resistance between Wx and Bx, is:

$$R_{WB}(D) = \frac{D}{2^N} \cdot R_{WB_FS} + R_W \qquad (1)$$

Where D is the decimal equivalent of the data contained in the RDAC register, $2^N$ is the number of steps, $R_{WB_FS}$ is the full scale resistance between terminals W-and-B, and $R_w$ is the wiper resistance.

For example, the following output resistance values will be set for the following RDAC latch codes (applies to $R_{WB_FS}$=25KΩ programmable resistors):

| D (DEC) | $R_{WB}(D)$ (Ω) | Output State |
|---|---|---|
| 1023 | 25026 | Full-Scale |
| 512 | 12550 | Mid-Scale |
| 1 | 74.4 | 1 LSB |
| 0 | 50 | Zero-Scale (Wiper contact resistance) |

Note that in the zero-scale condition a finite wiper resistance of 50Ω is present. Care should be taken to limit the current flow between W and B in this state to no more than 20mA to avoid degradation or possible destruction of the internal switches.

The typical distribution of full scale $R_{WB}$ from channel-to-channel matches to ±0.2% within the same package. Device to device matching is process lot dependent with the worst case of ±30% variation. On the other hand, the change in $R_{WB}$ with temperature has a 35ppm/°C temperature coefficient.

**TEST CIRCUITS**

Figures 10 to 12 show some of the test conditions used in the product specification table.

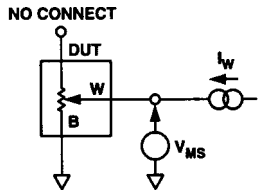



Figure 10. Resistor Position Nonlinearity Error (Rheostat Operation; R-INL, R-DNL*)*

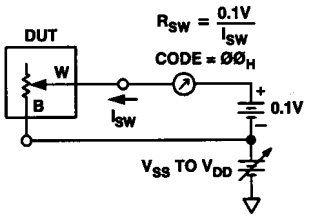



Figure 11. Incremental ON Resistance Test Circuit

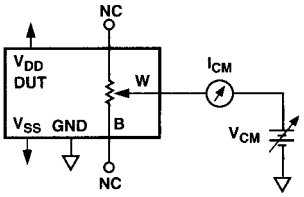



Figure 12. Common Mode Leakage current test circuit

**PROGRAMMING EXAMPLES**

The following programming examples illustrate typical sequence of events for various features of the ADN2850. Users should refer to Table 2 for the instructions and data word format. The Instruction numbers, addresses, and data appearing at SDI and SDO pins are based in hexadecimal in the following examples.

| SDI | SDO | Action |
|---|---|---|
| $B00100_H$ | $XXXXXX_H$ | Loads data $100_H$ into RDAC1 register, Wiper W1 moves to 1/4 full-scale position |
| $B10200_H$ | $B00100_H$ | Loads data $200_H$ into RDAC2 register, Wiper 2 moves to 1/2 full-scale position |

Example 1. Set two programmable resistors to independent data

| SDI | SDO | Action |
|---|---|---|
| $B00100_H$ | $XXXXXX_H$ | Loads data $100_H$ into RDAC1 register, Wiper W1 moves to 1/4 full-scale position |
| $E0XXXX_H$ | $B00100_H$ | Increments RDAC1 register by one to $101_H$ |
| $E0XXXX_H$ | $E0XXXX_H$ | Increments RDAC1 register by one to $102_H$ |
| Continue until desired wiper position reached | | |
| $20XXXX_H$ | $XXXXXX_H$ | Saves RDAC1 register data into EEMEM1 |
| Optionally tie WP to GND to protect EEMEM values | | |

Example 2. Incrementing one programmable resistor followed by storing the wiper setting to EEMEM

| EEMEM values for RDACs can be restored by | | |
|---|---|---|
| Power On or | | |
| Strobing PR pin or | | |
| Programming shown below | | |
| SDI | SDO | Action |
| $10XXXX_H$ | $XXXXXX_H$ | Restores EEMEM1 value to RDAC1 register |
| $00XXXX_H$ | $10XXXXX_H$ | NOP. Recommended step to minimize power consumption |
| $8XXXXX_H$ | $00XXXX_H$ | Restores EEMEM1 and EEMEM2 values to RDAC1 and RDAC2 registers respectively |

Example 3. Restoring EEMEM values to RDAC registers

| SDI | SDO | Action |
|---|---|---|
| $C0XXXX_H$ | $XXXXXX_H$ | Moves wiper #1 to double the present data contained in RDAC1 register |
| $C1XXXX_H$ | $C0XXXX_H$ | Moves wiper #2 to double the present data contained in RDAC2 register. |

Example 4. Using Left shift by one to increment +6dB steps

| SDI | SDO | Action |
|---|---|---|
| $32AAAA_H$ | $XXXXXX_H$ | Stores data $AAAA_H$ into spare EEMEM location USER1 (Allowable to address in 13 locations with maximum 16-bits of Data) |
| $335555_H$ | $32AAAA_H$ | Stores data $5555_H$ into spare EEMEM location USER2. (Allowable to address 13 locations with maximum 16-bits of Data) |

Example 5. Storing additional user data in EEMEM

| SDI | SDO | Action |
|---|---|---|
| $92XXXX_H$ | $XXXXXX_H$ | Prepares data read from USER1 location |
| $00XXXX_H$ | $92AAAA_H$ | NOP instruction #0 sends 24-bit word out of SDO where the last 16 bits contain the contents of USER1 location. NOP command insures device returns to idle power dissipation state |

Example 6. Reading back data from various memory locations

| SDI | SDO | Action |
|---|---|---|
| $B00200_H$ | $XXXXXX_H$ | Sets RDAC1 to mid-scale |
| $C0XXXX_H$ | $B00200_H$ | Doubles RDAC1 from mid-scale to full scale |
| $A0XXXX_H$ | $C0XXXX_H$ | Prepares reading wiper setting from RDAC1 register |
| $XXXXXX_H$ | $A003FF_H$ | Readback full scale value from RDAC1 register. |

Example 7. Reading back wiper setting

Analog Devices offers a user friendly ADN2850EVAL evaluation kit and it can be controlled by a personal computer through the printer port.

## APPLICATIONS

### Optical Transmitter Calibration with ADN2841

Together with the multi-rate 2.7Gbps Laser Diode Driver ADN2841, the ADN2850 forms an optical supervisory system where the dual programmable resistors can be used to set the laser average optical power and extinction ratio, see Figure 13. ADN2850 is particularly ideal for the optical parameter settings because of its high resolution and superior temperature coefficient characteristics.

The ADN2841 is a 2.7 Gbps laser diode driver that utilizes a unique control algorithm to manage both the laser average power and extinction ratio after the laser initial factory calibration. It stabilizes the laser data transmission by continuously monitoring its optical power, and correcting the variations caused by temperature and the laser degradation over time. In ADN2841, the $I_{MPD}$ monitors the laser diode current. Through its dual loop Power and Extinction Ratio control, calibrated by ADN2850, the internal driver controls the bias current $I_{BIAS}$ and consequently the average power. It also regulates the modulation current, $I_{MODP}$ by changing the modulation current linearly with slope efficiency. Any changes in the laser threshold current or slope efficiency are therefore compensated. As a result, this optical supervisory system minimizes the laser characterization efforts and therefore enables designers to apply comparable lasers provided from multiple sources.

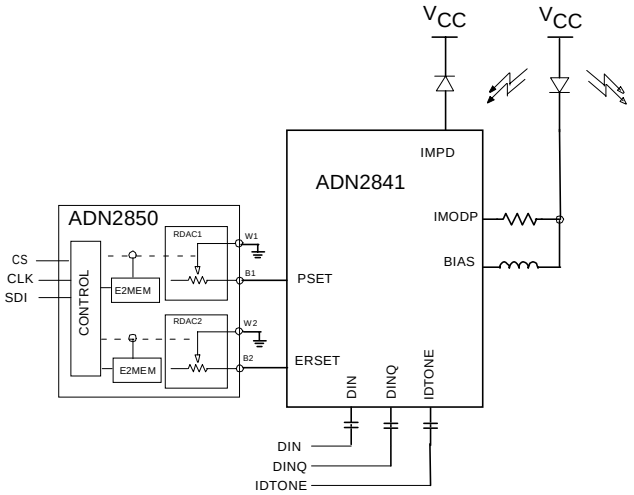



Figure 13. Optical Supervisory System

### Incoming Optical Power Monitoring

ADN2850 comes with a pair of matched diode-connected PNPs, $Q_1$ and $Q_2$, which can be used to configure an incoming optical power monitoring function. Figure 14 shows such conceptual circuit. With a reference current source, an instrumentation amplifier, and a logarithmic amplifier, this feature can be used to monitor the optical power by knowing the DC average photo diode current from the following properties:

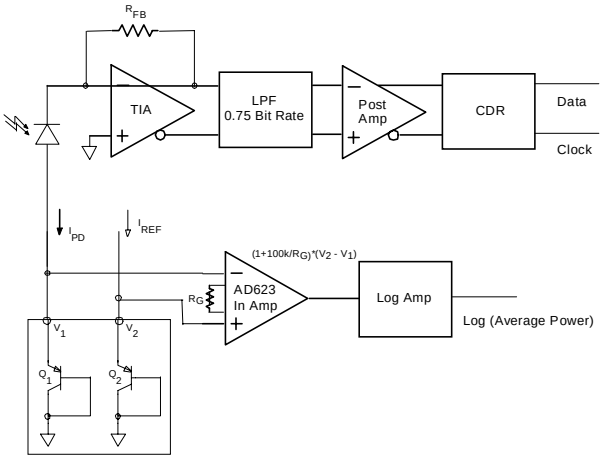



Figure 14. Conceptual Incoming Optical Power Monitoring Circuit.

$$V_1 = V_{BE1} = V_T \ln\frac{I_{C1}}{I_{S1}} \quad (2)$$

$$V_2 = V_{BE2} = V_T \ln\frac{I_{C2}}{I_{S2}} \quad (3)$$

Note $I_{C1} = \alpha_1 * I_{PD}$, $I_{C2} = \alpha_2 * I_{REF}$. Since $Q_1$ and $Q_2$ are matched, therefore $\alpha_1$ equals $\alpha_2$ and $I_{S1}$ equals $I_{S2}$. Combining equations 2 and 3 yields

$$V_1 - V_2 = V_T \ln\left(\frac{I_{PD}}{I_{REF}}\right) \quad (4)$$

Where $I_{S1}$ and $I_{S2}$ are saturation current
$V_1$, $V_2$ are $V_{BE}$, base-emitted voltages of the diode-connector transistors
$V_T$ is the thermal voltage which is equal to k*T/q. $V_T$=26mV at 25°C
k = Boltzmann's constant = 1.38E-23 joules/kelvin
q = electron charge = 1.6E-19 coulomb
T = temperature in kelvin
$I_{PD}$ = photo diode current
$I_{REF}$ = reference current

With the final logarithmic amplification, the output voltage represents the average incoming optical power. The output voltage of the log stage does not have to be accurate from device to device as the responsivity of the photo diode will change. However, temperature compensation and the aging stability of the photo diode may be required. The user may also calibrate the log amp using two values of input optical power to give an offset and gradient values. This negates the need for a true log base 10 conversion.

### Resistance Scaling

ADN2850 offers either 25KΩ or 250KΩ full scale resistance. For users who need lower resistance and still maintain the numbers of step adjustment, they can parallel multiple devices. Figure 15 shows a simple scheme of paralleling both channel of the RDACs. In order to adjust half of the resistance linearly per step, users need to program the RDACs coherently with the same settings and tie the terminals as shown. Much lower

resistance can also be achieved by paralleling a discrete resistor as shown in Figure 16. The equivalent resistance at a given setting is approximated as

$$R_{eq} = \frac{D \cdot R_{WB_FS} + 51200}{D \cdot R_{WB_FS} + 51200 + 1024 \cdot R} \quad (5)$$

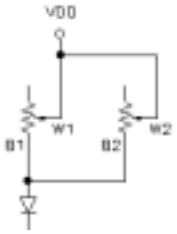



Figure 15. Reduce Resistance by half with linear adjustment characteristics

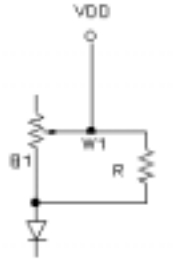



Figure 16. Resistor Scaling with log adjustment characteristics

In this approach, the adjustment is not linear but logarithmic. Users should also be aware the need for tolerance matching as well as temperature coefficient matching of the components.

**BASIC RDAC SPICE MODEL**

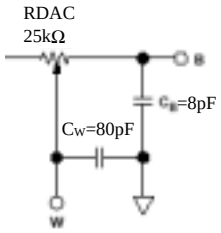



Figure 17. RDAC Circuit Simulation Model for RDAC = 25 kΩ

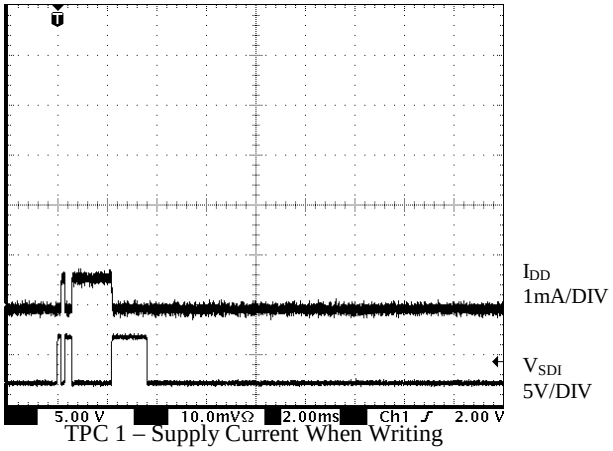
The internal parasitic capacitances and the external capacitive loads dominate the ac characteristics of the RDACs. A general parasitic simulation model is shown in Figure 7. Listing I provides a macro model netlist for the 25 kΩ RDAC:

**Listing I. Macro Model Net List for RDAC**

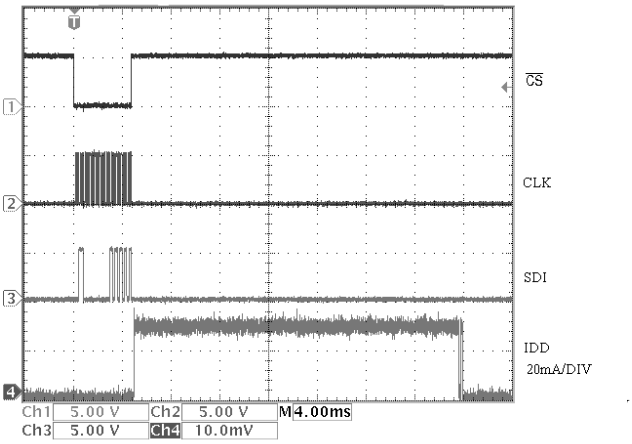
```
.PARAM D=1024, RDAC=25E3
*
.SUBCKT RDAC (W,B)
*
RWB  W B {D/1024*RDAC+50}
CW   W 0 80E-12
CB   B 0 8E-12
*

.ENDS RDAC
```

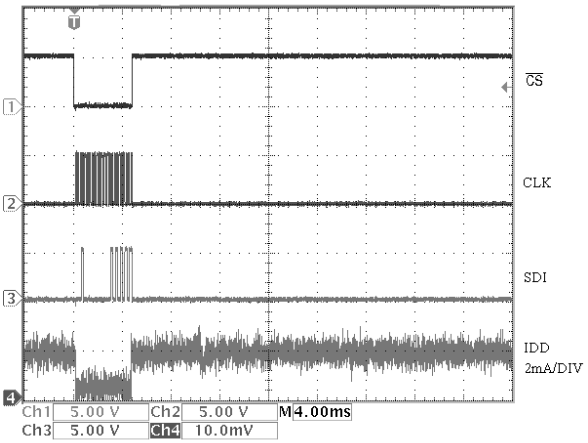
**ADN2850 – Typical Performance Characteristics**




TPC 1 – Supply Current When Writing Data to RDAC




TPC 2 – Supply Current in Storing Data to $E^2$MEM

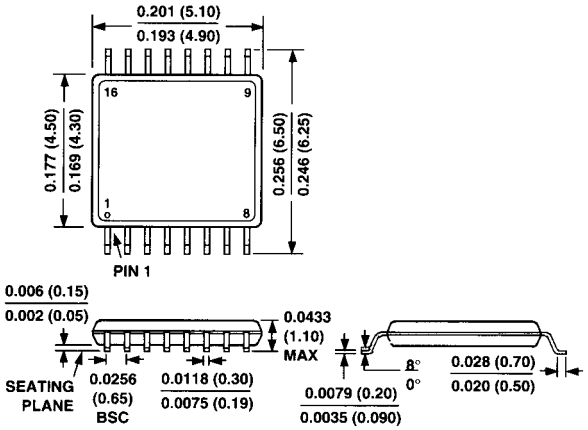



TPC 3 – Supply Current in Retreiving Data from $E^2$MEM

**OUTLINE DIMENSIONS**

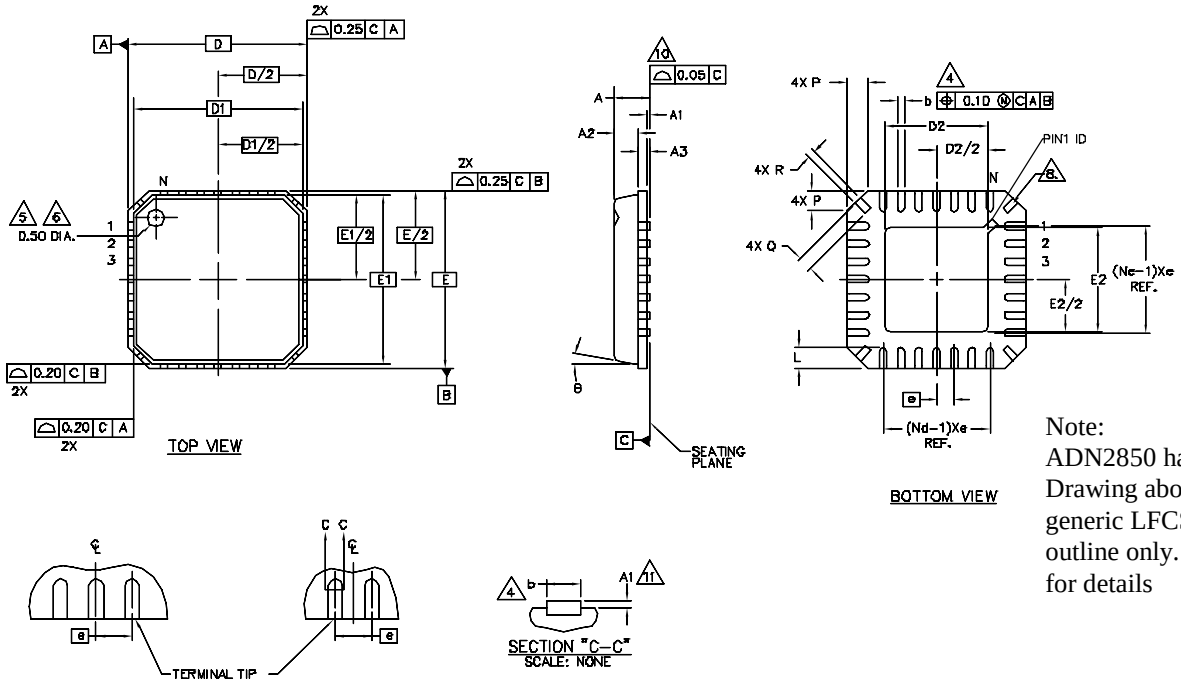
Dimensions shown in inches and (mm)

**16-Lead TSSOP**
**(RU-16)**



# Nonvolatile Memory Programmable Resistors ADN2850

**16-Lead LFCSP 5mm x 5mm (CP-16)**




Note:
ADN2850 has 16 pins. Drawing above illustrates a generic LFCSP package outline only. Please see table for details

FOR ODD TERMINAL/SIDE FOR EVEN TERMINAL/SIDE

| SYMBOL | PITCH VARIATION A MIN. | NOM. | MAX. | NOTE |
|---|---|---|---|---|
| e | | 0.80 BSC | | |
| N | | 16 | | 3 |
| Nd | | 4 | | 3 |
| Ne | | 4 | | 3 |
| L | 0.35 | 0.55 | 0.75 | |
| b | 0.28 | 0.33 | 0.40 | 4 |
| Q | 0.30 | 0.40 | 0.65 | |
| MO-220 | D2 | SEE EXPOSED PAD VARIATION: C | | |
| | E2 | SEE EXPOSED PAD VARIATION: C | | |
| | | VHHB (see note 12.) | | |

| SYMBOL | COMMON DIMENSIONS MIN. | NOM. | MAX. | NOTE |
|---|---|---|---|---|
| A | – | 0.85 | 1.00 | |
| A1 | 0.00 | 0.01 | 0.05 | 11 |
| A2 | – | 0.65 | 0.80 | |
| A3 | | 0.20 REF. | | |
| D | | 5.00 BSC | | |
| D1 | | 4.75 BSC | | |
| E | | 5.00 BSC | | |
| E1 | | 4.75 BSC | | |
| θ | | | 12° | |
| P | 0.24 | 0.42 | 0.60 | |
| R | 0.13 | 0.17 | 0.23 | |

| SYMBOLS | | D2 MIN | D2 NOM | D2 MAX | E2 MIN | E2 NOM | E2 MAX | NOTE |
|---|---|---|---|---|---|---|---|---|
| EXPOSED PAD VARIATIONS | A | 2.95 | 3.10 | 3.25 | 2.95 | 3.10 | 3.25 | |
| | B | 2.55 | 2.70 | 2.85 | 2.55 | 2.70 | 2.85 | |
| | C | 3.15 | 3.30 | 3.45 | 3.15 | 3.30 | 3.45 | |

NOTES:
1. DIE THICKNESS ALLOWABLE IS 0.305mm MAXIMUM(.012 INCHES MAXIMUM)
2. DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. – 1994.
3. N IS THE NUMBER OF TERMINALS.
   Nd IS THE NUMBER OF TERMINALS IN X-DIRECTION &
   Ne IS THE NUMBER OF TERMINALS IN Y-DIRECTION.
4. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25mm FROM TERMINAL TIP.
5. THE PIN #1 IDENTIFIER MUST BE EXISTED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR OTHER FEATURE OF PACKAGE BODY.
6. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
7. ALL DIMENSIONS ARE IN MILLIMETERS.
8. THE SHAPE SHOWN ON FOUR CORNERS ARE NOT ACTUAL I/O.
9. PACKAGE WARPAGE MAX 0.05mm.
10. APPLIED FOR EXPOSED PAD AND TERMINALS. EXCLUDE EMBEDDING PART OF EXPOSED PAD FROM MEASURING.
11. APPLIED ONLY FOR TERMINALS.
12. JEDEC MO-220 DESIGNATOR